REMARKS

Reconsideration of the present application as amended is respectfully requested. Claims 1 and 5 have been amended. Claims 1-6 are currently pending.

Claims 1 and 5 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,226,127 to Fu et al. ("Fu"). Regarding claims 1 and 5, the Office Action asserts that Figure 1 and column 6, lines 37-49 teach "first processor means which is operable to process instructions from a first set of instructions" and "second processor means which is operable to process instructions from a second set of instructions, which second set of instructions is a subset of the first set of instructions." The Office Action further asserts that column 6, line 36 to column 8, line 5 and Figure 1 of Fu teaches "the second processor means being arranged to receive instructions and to process the received instructions without reference to the first processor means, when the received instructions are selected from the second set of instructions." The Office Action still further asserts that column 3, lines 39-49 and Figure 1 of Fu teaches that "the first processor means includes a plurality of registers, and the second processor means is operable to access a predetermined, non-zero, selection of the said registers."

Independent claims 1 and 5 have been amended to each include the feature of "wherein the first and second processors are operable to process respective instructions in parallel with one another." Support for the amendments to independent claims 1 and 5 can be found at at least page 6, lines 18-23 of the application as originally filed. Applicant respectfully submits that Fu fails to teach or suggest at least these respective features of independent claims 1 and 5 as amended.

Fu describes the use of a synchronization instruction to cause a general purpose processor of a computer system to wait further processing of instructions until a special purpose processor of the computer system signals completion of processing (See, column 6, lines 36-48 of Fu). As such, Fu describes a computer system in which a general purpose processor and a special purpose processor operate in a mutually exclusive manner. In contrast, the invention of independent claim 1 as amended describes a processing arrangement wherein first and second processor means are operable to process respective instructions in parallel with one another. Applicant respectfully submits that this feature is not taught or suggested by Fu. Applicant

respectfully submits that independent claim 1 distinguishes over Fu and requests that the 35 U.S.C. 102(b) rejection of independent claim 1 be withdrawn.

As previously discussed, independent claim 5 has been amended to include the feature of "wherein the first and second processors are operable to process respective instructions in parallel with one another." For the same reasons as those discussed with respect to independent claim 1, Applicant respectfully submits that this feature of independent claim 5 is not taught or suggested by Fu. Applicant respectfully submits that independent claim 5 distinguishes over Fu and requests that the 35 U.S.C. 102(b) rejection of independent claim 5 be withdrawn.

Claims 2-4 and 6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Fu in view of U.S. Patent No. 5,614,847 to Kawahara et al. ("Kawahara"). With respect to claims 2 and 6, the Office Action acknowledges that Fu does not teach "an arrangement as claimed in claim 1, wherein the first processor means has active and inactive states of operation, and wherein the second processor means is operable to process instructions when the first processor means is in the inactive state." The Office Action asserts that column 31, lines 25-38 of Kawahara teaches "wherein the first processor means has active and inactive states of operation, and wherein the second processor means is operable to process instructions when the first processor means is in the inactive state." The Office Action further asserts that "allowing the coprocessor to have active and inactive states would have been obvious to one of ordinary skill in the art at the time of the invention" because "by having the first processor, or coprocessor, in a sleep state, less power is dissipated so that the system uses less total power."

Claims 2-4 and 6 are dependent upon and include the features of their respective independent claims 1 and 5. As discussed with respect to independent claims 1 and 5, Fu fails to teach or suggest the feature of "wherein the first and second processors are operable to process respective instructions in parallel with one another." Kawahara describes an integrated circuit that may be used in devices having both an operation mode and a sleep mode used for power reduction. Column 31, lines 25-38 describes a co-processor COPA 602 and a co-processor COPB 603 in which the individual co-processors are in a sleep state before execution of their respective instructions are started, so that little power is dissipated. Applicant respectfully submits that Kawahara also appears to contain no teaching or suggestion of the aforedescribed

feature of independent claims 1 and 5 of " wherein the first and second processors are operable to process respective instructions in parallel with one another." Applicant respectfully submits that claims 2-4 and 6 distinguish over Fu in view of Kawahara and requests that the 35 U.S.C. 103(a) rejection of claims 2-4 and 6 be withdrawn.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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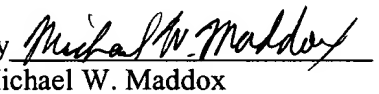
Respectfully submitted,

By 

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